Stacked Chip Thermal Model Validation using Thermal Test Chips

Thomas Tarter
Package Science Services
ttarter@pkgscience.com

Bernie Siegal
Thermal Engineering Associates, Inc.
bsiegal@thermengr.net

INTRODUCTION

Increasing demands on density, functionality and performance in small package footprints has lead to a higher market share for stacked-chip packaging. This trend has brought with it the need for better understanding of thermal issues associated with removing heat from the various chips in the stack. Typically, thermal simulation models are used to gain an insight to heat flow issues in complex multi-chip packages. The validity of the models and the assumptions drawn from the model results are questionable unless measurements are used to validate the model results.

Unfortunately, validation measurements are difficult to make on multiple-interconnected chips and, even if they can be made, often do not provide sufficient certainty and detail to accurately validate the model. For example, using the substrate isolation diode in an application chip will provide a junction temperature measurement. But that measurement is instead a weighted average of the temperatures across the chip and does not provide for any spatial resolution relative to the highest temperatures on the chip. This is of particular concern on large square chips and chips with a high X-Y aspect ratio. Thus, attempting to use measurement data in this case to validate a thermal model leads to less than ideal results. A similar issue with the application chip approach is determining the specific location, area and magnitude of the heater power (hot spot).

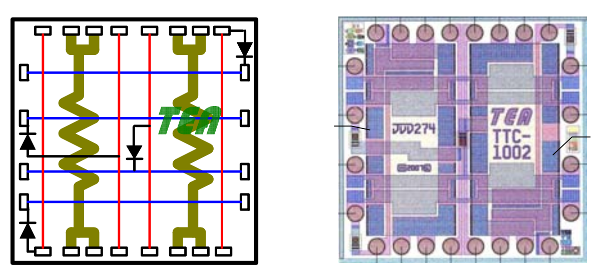
To address the problems with measurement of temperature in multi-chip packages a thermal test chip (TTC) has been developed and tested. The TTC is specifically designed to provide known locations for both temperature measurement and heat flux generation. Use of the TTC provides known power in specific spatial locations, thus making the model generation and validation easier and more accurate. Once a model is validated, the model can be varied to study heat flow and junction temperature under a variety of packaging approaches and environmental conditions. This presentation will deal with the application of TTCs in various configurations to demonstrate the ease and accuracy of thermal model development, generation and validation. Several model cases will be presented with validation data where available. At the time of publication, wire bonded stacked chip samples were available. Flip-chip studies will be presented at a later date.

Nomenclature

T_J	junction temperature
T_{JMAX}	maximum junction temperature
T_A	ambient temperature, °C
T_R	reference temperature, °C or K
P_D	power dissipation, W
θ_{JA}	thermal resistance, junction to ambient, °C/W
K_F	K factor, °C/mV
k	thermal conductivity, W/mK
h	convection heat transfer coefficient, W/m^{2}K
WB	wire bond
FC	flip-chip
TTC	thermal test chip
I_M	measurement current, A
V_M	measurement voltage, V
I_H	heating current, A
V_H	heating voltage, V
BGA	ball-grid-array
PCB	printed circuit board
TTB	thermal test board

Thermal Test Chip

The study described here uses a specialized test chip developed and manufactured by Thermal Engineering Associates. The basic unit cell is 2.54mm x 2.54mm in size. A schematic representation of a unit cell and an image of the chip layout are shown in Figure 1. Unit cells can be arrayed into larger chips by selective sawing to square or rectangular patterns in 2.54mm increments. Each unit cell has two metal film resistors for heat flux generation and four PN Junction diodes for temperature sensing. Figure 2 shows an example of a 2x2 array with electrical connections. The test chips are available in either wire-bond (WB) or flip-chip (FC) versions.



Chip Schematic Chip Layout

Figure 1.Thermal Test Chip TTC-1002

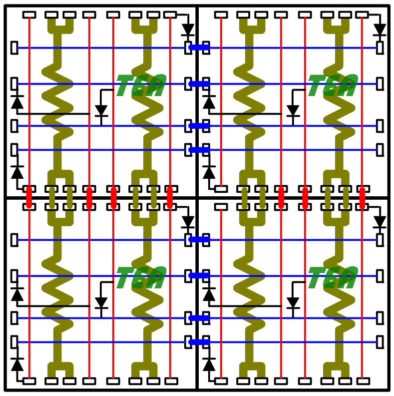


Figure 2. 2x2 TTC Array

Experimental Matrix and Sample Details

Two ball grid array substrate designs were generated for experiment; wire-bond and flip-chip interconnect. The substrate routing allows a single 2x2 array for WB or FC and connections for a second single unit cell mounted on top of the FC or WB base chip. Package details are shown in Table 1. Four different package constructions were assembled for experimental evaluation. Table 2 shows the configuration details. Figure 3 shows solid models of the four package types. Note: Wire bond pads exist for the top chip on packages 2a and 2b but are not shown in these diagrams. In addition, polycarbonate lids are attached after bonding to protect the chip and wire bond assembly.

Table 1. Package Details

Substrate material:	High Temperature FR-4
Substrate size:	12.7mm X 12.7mm
Ball pitch:	0.8mm
Ball size:	0.5mm Ø
Ball Array:	15X15 partially filled
Ball configuration:	201 balls with 5X5 thermal array in center
Chip Protection:	Polycarbonate shell

Table 2. Sample Configurations

Configuration	Chip Bottom	Chip Top
1-a	5.08mm x 5.08mm WB	NA
1-b	5.08mm x 5.08mm WB	2.54mm x 2.54mm WB
2-a	5.08mm x 5.08mm FC	NA
2-b	5.08mm x 5.08mm FC	2.54mm x 2.54mm WB

Each version of the package was mounted on a separate universal Thermal Test Board (TTB). The TTB, shown in Figure 4, was designed in general conformance to the JEDEC JESD51-5 standard. However, the board design allows for various wiring connection configurations so that different heat flux generation patterns can be investigated. Temperature measurements under these patterns can be made at multiple locations on the chip.

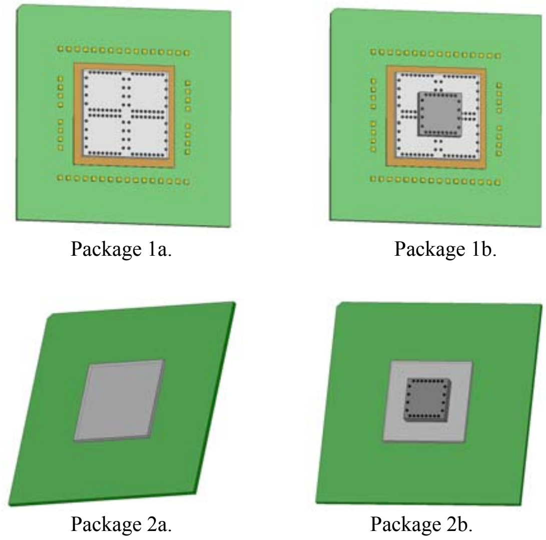


Figure 3. Sample Configurations

Figure 4. Thermal Test Board (TTB)

Measurements

The thermal test chip unit cell has two metal film resistors for heat flux generation and four PN junction diodes for temperature sensing. Package configuration 1a and 1b are used for measurement samples in this study. The measurement procedure for single and multi-chip packages is similar. Measurements performed on the 1a sample single-chip package uses the wiring diagram in Figure 5a. The 1b sample two-chip package uses the schematic shown in Figure 5b. Figure 5a shows how a 2x2 array of unit cells can be interconnected to produce a single resistor value of 3.8Ω.

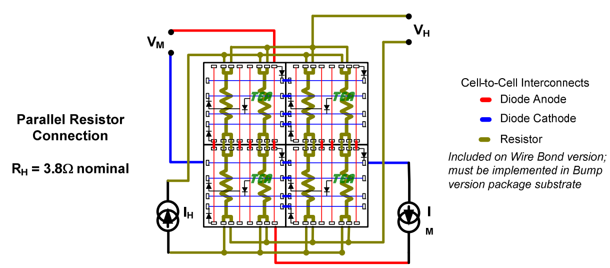


Figure 5a. 1a Sample Schematic and Biasing

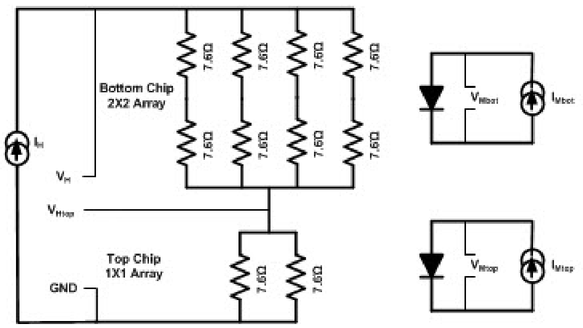


Figure 5b. 1b Sample 2-chip Schematic and Biasing

The stacked package top chip is a unit cell with resistors wired in parallel to produce the same resistance value of 3.8Ω. Kelvin (4-wire) connections to the array center diodes are made by wire bonding to the appropriate periphery pads on the top and bottom chips. Figure 6 shows the bond diagram for the 1b test sample and an isometric view of the die stack. The single chip 1a sample is identical, but without the top chip and wire bonds.

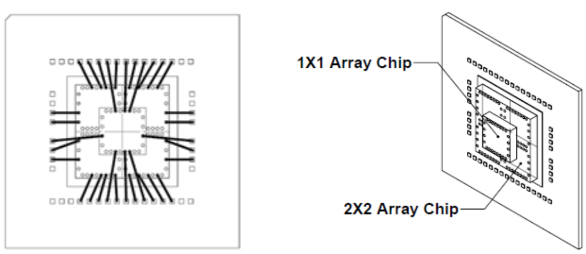


Figure 6. Sample 1b Bond Diagram and Die Stack

To insure the highest measurement accuracy, the diode is calibrated by inserting the chip, package and thermal test board assembly into a temperature-controlled environment and applying a 1mA measurement current (IM) to the diode. Monitoring the diode voltage over the temperature range of approximately 25ºC to 100ºC produces a K Factor value of 0.5234ºC/mV. The thermal test board assembly is inserted into a JEDEC JESD51-2 Natural Convection (Still Air) compliant environment. A Heating Current (I_H) is applied to produce approximately 1W of total heat flux. For the 1a sample, the power dissipation is distributed across the surface of the 2x2 array. The 1b sample heat flux is roughly evenly divided to 0.5W across each of the bottom and top chips. Monitoring the diode and resistor voltages over the range of 1ms to 2,000 seconds produces the thermal resistance heating curve. The result for sample 1a is shown in Figure 7a. The steady-state condition at 1,000 seconds resulted in an average value of 54.7ºC/W. Sample 1b measurements require monitoring two diode temperature sensors; one for each chip. The average steady-state thermal resistance for the two-chip package can be defined as the maximum measured rise in temperature divided by the total power dissipation as shown in Equation 1. For the 1b sample, the measurement result using equation 1 is 69°C/W.

Equation 1. $$\theta_{JA} = \frac{T_{J\max} - T_A}{P_{d_{TOTAL}}}$$

Where: T_{Jmax} is the highest temperature measured in the package and P_d is the total power dissipated in the chips.

The value derived from Equation 1 is a standard metric for a single chip package, but may be less useful in a multi-chip package; the location of the maximum temperature point is unknown. In the case of the test chips, the temperature sensor is located near the center of the unit cell or array at the assumed peak temperature point. This assumption holds true for cases where the power dissipation is distributed evenly across the chip(s). For real devices this may not be the case. Hot spots may exist on chips in the stack and care must be taken to avoid aligning areas that may have higher power dissipation than surrounding circuits on the same chip. Because silicon is a good thermal conductor, spreading of heat in the chip decreases temperature gradients, but hot spot alignment in stacks can be a key failure mechanism. To further refine thermal resistance for the 1b sample, the value may also be defined as the maximum temperature rise for each chip divided by the total power dissipated. Equations 2a and 2b show examples.

Eq. 2a $$\theta_{JA} = \frac{T_{Jtop} - T_A}{P_{d_{TOTAL}}}$$ Eq. 2b $$\theta_{JA} = \frac{T_{Jbot} - T_A}{P_{d_{TOTAL}}}$$

The use of these equations help to determine individual chip temperatures, however, the chips in a stacked arrangement are thermally coupled so this value will vary dependent on power distribution across both chips. Figure 7b shows the heating curve for the top chip in the 1b package using Eq. 2a. The result is 69.1°C/W. The bottom chip array thermal resistance measured 66.8°C/W. Table 3 lists a summary of the measurement experiments.

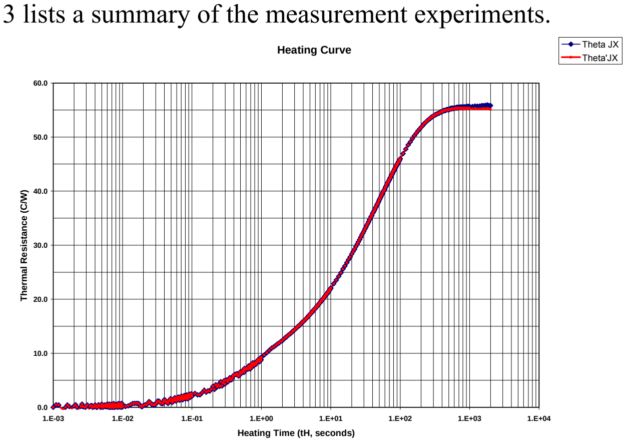


Figure 7a. Configuration 1a Heating Curve

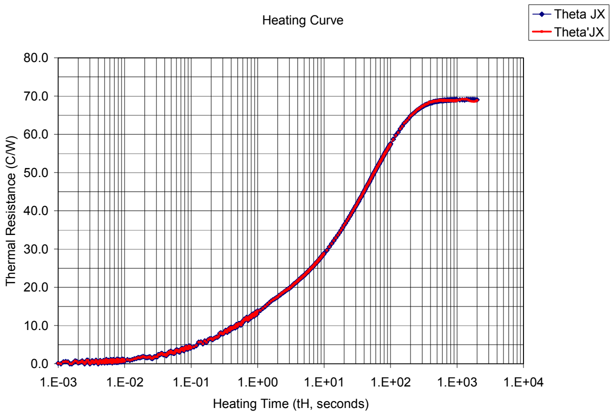


Figure 7a. Configuration 1b Heating Curve (top chip)

Table 3. Measurement Results

	Tjmax		θ_{JA} (°C/W)	
Config.	2x2	1x1	2x2	1x1
1a	90.74	NA	54.7	NA
1b	109.27	111.85	66.8	69.1

Package Thermal Models

Developing models for the thermal test chip with full validation provides an excellent methodology for prediction of various configurations of chip geometry, physical arrangement, temperature distribution (hot spots) and environmental effects. The data from the test chip models and measurements can be extended to real-world applications by utilizing thermal load boards with packaged thermal test chips designed to mimic products in development. This allows much faster thermal design as the thermal engineer does not have to wait for full development of the production chip and board to find an optimal solution. Validated models can be extended to variations to perform inexpensive 'what-ifs' and optimization studies. The models in this presentation use the finite-element method

FEM thermal models were generated in tandem with measurements. These models include all geometric, materials and interface details of the packaged chip and board. Table 4 shows the materials in the assembly.

Table 4. Package and PCB Materials

Component	Material
Lid	Polycarbonate
Wire Bond	Aluminum, 1/% Si .00125" dia.
Top Chip	Silicon
Bottom Chip	Silicon
Die Attach (bot)	Hysol JM700 .0025 bond line
Die Attach (top)	Hysol e-60nc .0025 bond line
Substrate	FR-4
Ball Array	SAC 305
PCB	FR-4

Package Model Details

The model includes

- 12.7mm square BGA
- Single chip: 5.08x5.08mm
- Two stacked chips: 5.08x5.08mm and 2.54x 2.54mm square, 300um thick
- Aluminum wire bonds from both chips to substrate
- Die attach layers represented by contact resistance
- Polycarbonate lid
- 100mm (4") square PCB coupon

Geometric simplifications are required to allow reasonable aspect ratios for high-quality meshing and well converged solutions. Some features modified in this model include simplification of the PCB and package substrate, the use of rectangular shapes for bond wires, solder columns instead of spheres and contact resistance boundary conditions for the die attach layers. Figure 8 shows an exploded view of the solid model.

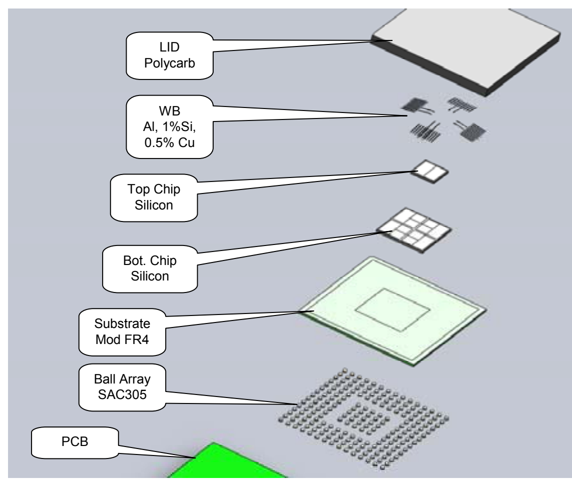


Figure 8. Exploded View (2-chip model)

PCB and BGA Substrate Models

The PCB model uses high-temperature FR-4 glass-epoxy material properties. The board is considered to be low thermal conductivity and has a 2S0P stack up. The board is .032in thick with 2oz Cu sparsely placed traces (see Figure 4). The PCB has a 4 x 4 array of thermal vias with 0.2in plated through holes connected to 0.16" x 0.16" planes on the top and bottom sides of the substrate. The board was simplified by solving models of the via array section with real geometry for via and plane plating through the FR-4 board. The model was solved to find heat flow characteristics and extract orthotropic thermal conductivity. The calculated thermal conductivities are used to create a new pseudo-material that represents heat flow through the real structure. The new material set is validated by comparison to the full model. The remainder of the PCB uses typical FR-4 material properties with the newly created material inserted into the center of the PCB as shown in Figure 9. The BGA substrate is modeled in a similar manner.

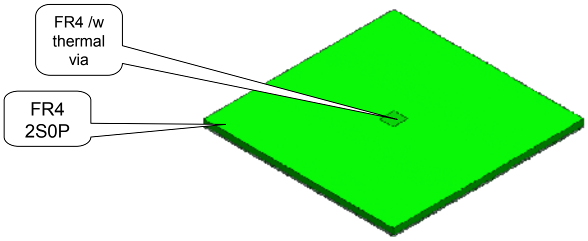


Figure 9. Composite PCB model

Chip Models

The 1a model uses a single 2x2 array. For the 1b model two chips are used stacked 'wedding cake' style with the unit cell attached to the 2x2 array base die with non-conductive die-attach material. The base die is attached to the BGA substrate with silver-filled epoxy die attach material. Each unit cell has metal film resistors which cover ~86% of the area of the chip. The model geometry places heat dissipating areas on the chip solids on the top surface approximating the actual size of the manufactured chip. There are two discrete resistor areas on a unit cell yielding 8 areas on the 2x2 array. Figure 10 shows the areas designated for power dissipation on the chip models.

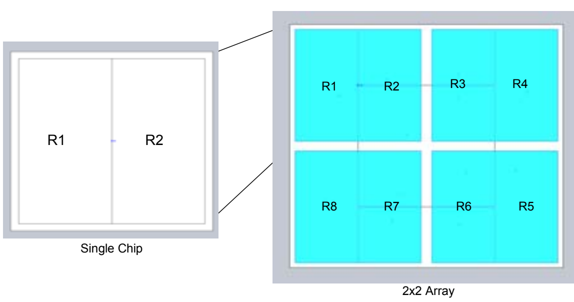


Figure 10. Chip Power Dissipation Areas

Interconnect

Wire bonds are modeled as rectangular bars with the same volume as the round wire used for assembly. The solder balls on the BGA package are modeled as solder columns with the same volume as the spherical balls used in assembly. Figure 11 shows a typical wire bond solid (a.) and a view of the solder columns (b.).

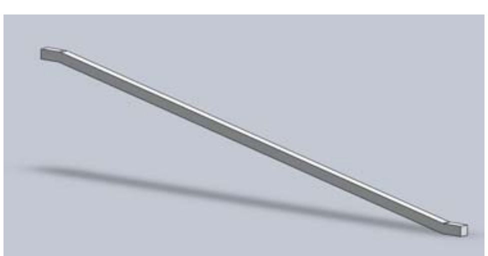


Figure 11a. Wire bond model representation

Figure 11b. Solder ball model representation

The model components were mated into an assembly. Figure 12 shows a cross-section view of the package model.

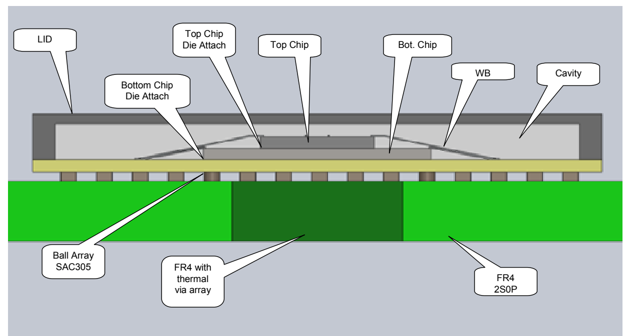


Figure 12. 1b Package Model Cross-section

Boundary Conditions

All model solutions were run at the measurement ambient temperature initial conditions. Die attach layers are simulated by contact resistance boundary conditions:

Bottom chip D/A $k = 2.7$W/mK, 2.5 mil thick 0.91 K/W
Top chip D/A $k = 2$ W/mK, 2.5 mil thick 4.92 K/W

Natural convection is simulated by applying convection heat transfer coefficients to the exposed surfaces of the model. Cut lines are used to avoid convection on mated surfaces. Note that the chip cover does not contact chip but is a hollow lid creating a cavity around the chip and wire bonds.

Heat is generated by applying power dissipation to the areas listed in the *Chip Model* section. Power dissipation was set to the values used during measurement.

Mesh

The mesh is generated using an automatic iterative meshing algorithm. The mesh engine generates parabolic tetrahedral solid elements. Due to the large aspect ratio of component geometry in the model, the mesh was refined in some areas to compensate for small geometry and transition to larger mesh elements. Mesh refinement includes wire bonds, chips, package substrate and lid. The final mesh contains ~140k elements and ~240k Figures 13a, b and c show the mesh results and refined areas.

Solution

The solution was solved using an FFE iterative solver to a steady-state condition. The program was run on an i7

Core processor running at 4.2Ghz with 16GB DDR running at 1.6GHz, Sandybridge chipset on MSI military motherboard with a liquid-cooled processor heat sink and a high performance Open GL workstation video card. The solution converges in ~ 30 seconds. Figure 14a and 14b show typical temperature distribution results at the board and at the chip level respectively.

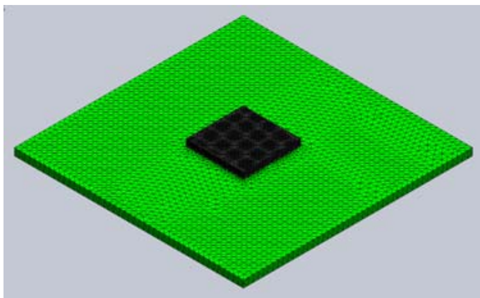


Figure 13a. Model Mesh

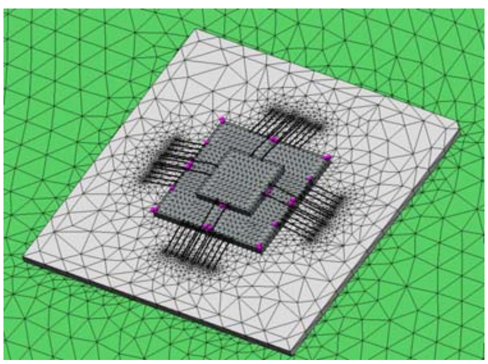


Figure 13b. Mesh Refinement

Figure 13c. Wire Bond Mesh

Results

Solutions show consistent results with normal temperature distribution. Distinct temperature steps can be seen at the chip-to chip and chip-to board interfaces due to the use of boundary conditions to represent die attach layers. Figure 14a shows the temperature contour plot with the lid removed. Figure 14b shows the temperature profile horizontally across the center of the array. The single-chip model results show a maximum temperature of 92.1°C corresponding to a thermal resistance of 56.7°C/W.

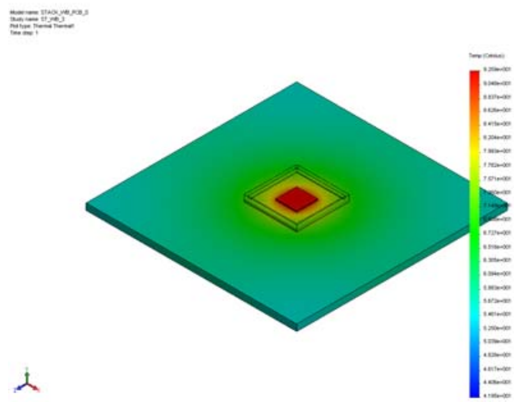


Figure 14a. 1a Model Temperature Contour

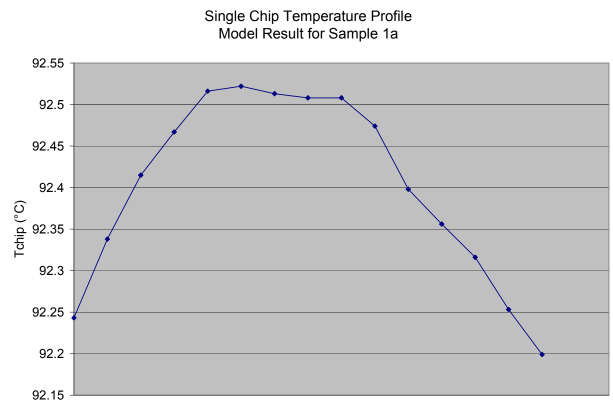


Figure 14b. 1a Chip Temperature Profile

For the 1b, two-chip model, the solution was run using the standard material set and boundary conditions described previously. This first model is termed the "Base Model" and will be used as a reference for case studies. The Base Model solution resulted with a maximum chip temperature (T_{JMAX}) of 112.4°C located on the top chip. Because the lid material does not contact the chips heat is only transferred by small convection currents within the cavity. Top chip thermal resistance, junction to ambient (θ_{JA}) is calculated using Equation 2a resulting in a value of 69.1°C/W. Bottom chip solution T_{JMAX} result is 110.2°C in the center of the bottom chip surface yielding a thermal resistance of 66.8°C/W.

Figure 15a shows the contour plot for the 1b sample with the lid removed. Figure 15b shows a cross-section of the solution plotted with the temperature contour. This plot indicates that spreading in the low thermal conductivity FR4 PCB is minimal. The primary conduction heat flow is through the higher thermal conductivity via array in the PCB center.

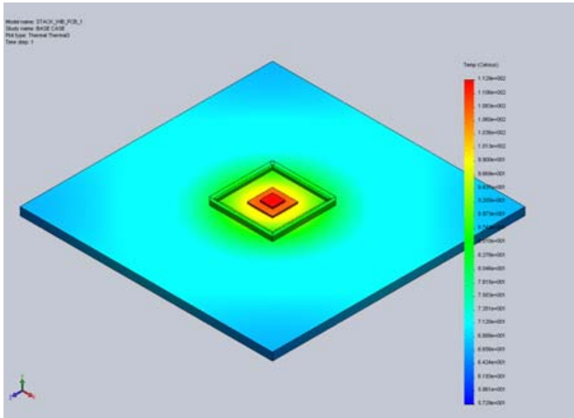


Figure 15a. 1b Model Temperature Contour

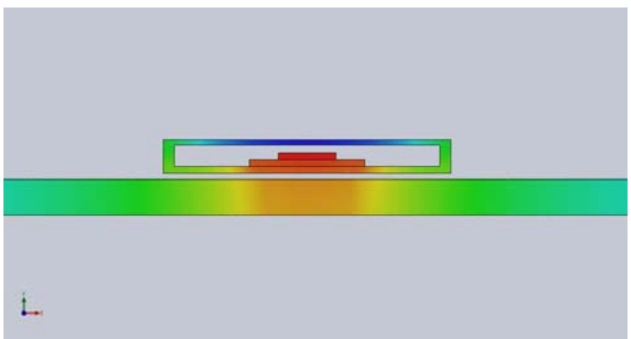


Figure 15b. 1b Model Cross-section Contour Plot

Comparison to Measurements

Comparing the result to the measurements, we find that the solution, using standard boundary conditions, is well within experimental and tolerance error bounds and is usable as a reference model for the assembly. Table 5 lists the model and measurement results and the error percentage for T_{JMAX} and θ_{JA} using the measurement value as a reference. The validated base model can be used to evaluate changes in variables on the result with good confidence.

Table 5. Measurement and Model Comparison

°C	Tjmax - Measure		Tjmax - Model		Tjmax - Error	
Config.	2x2	1x1	2x2	1x1	2x2	1x1
1a	90.74	NA	92.1	NA	1.5%	NA
1b	109.27	111.85	110.2	112.4	0.8%	0.5%
°C/W	θ_{JA} Measure		θ_{JA} - Model		θ_{JA} - Error	
Config.	2x2	1x1	2x2	1x1	2x2	1x1
1a	54.7	NA	56.2	NA	2.7%	NA
1b	66.8	69.71	67.6	69.0	1.2%	-1.0%

Model Test Cases

Several model cases were solved with variations in power distribution to show the effects on T_{JMAX} and temperature distribution. Case study model results use the Base Model result as a reference. The power distribution study varies power dissipation on each chip by concentrating power in the elements in a corner of the die to simulate hot spots and stacked hot spots. The four models take into consideration conditions that may be validated using the TTC by placing various heat sources on sections of the model corresponding to the chip thin-film resistor layout. All case studies use a total power of 1W. Table 6 lists the model case parameters for power distribution scenarios. Contour plots are scaled to the maximum and minimum temperatures for the given result set.

Table 6. Power Dissipation Case Studies

Name	Case No.	Top Chip Pd	Bot Chip Pd
Base Case	0	R1=R2=0.25W	R1-R8=0.0625W
Top Case	1	R1=0.4W R2=0.1W	R1-R8=0.0625W
Bottom Case	2	R1=R2=0.5W	R2=0.4W R1, R3-8=0.014W
Both Case	3	R1=0.4W R2=0.1W	R2=0.4W R1, R3-8=0.014W

Base Case

Figure 16 shows the power distribution map and resulting temperature distribution solution for the Base Case.

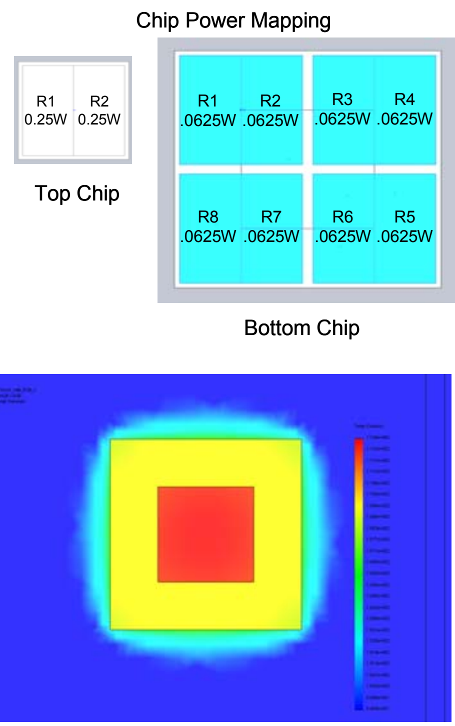


Figure 16. Base Case Power Map and Contour Plot

Top Case

This case simulates a hot spot on the top die by concentrating the power in the R1 area. The power map and temperature distribution are shown in Figure 17. Note that the concentration of power on the top die has a small effect on the maximum temperature. As will be seen later, in the report there is an effect on the temperature distribution at steady state. This is primarily due to the relatively high thermal conductivity of silicon. The maximum temperature for this model case is 112.8°C.

Bottom Case
This case simulates a hot spot on the bottom die by concentrating the power in the R2 area. The power map and temperature distribution is shown in Figure 18. Note that the concentration of power on the bottom chip has little effect on the maximum temperature of the assembly but has a significant affect on the bottom chip temperature. Tmax result for this model is 112.84C located on the top chip.

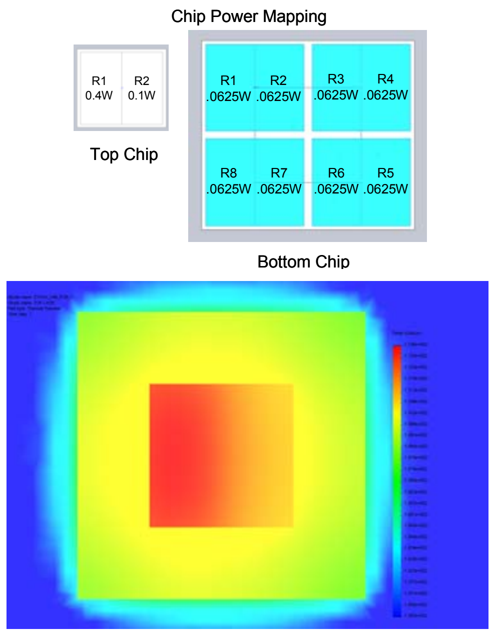


Figure 17. Top Case Power Map and Contour Plot

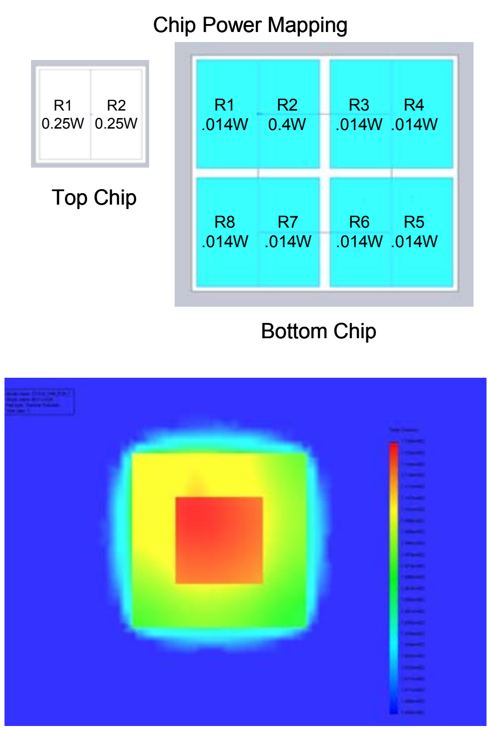


Figure 18. Bottom Case Power Map and Contour Plot

Both Case
This case simulates a hot spot on the bottom and top chips by concentrating the power in the R2 area of the bottom chip and the R1 area of the top chip. The power map and temperature distribution is shown in Figure 19. In this case the maximum temperature and the temperature distribution are affected. Tmax for this solution is 113.6°C.

Summary of Case Studies
Table 7 lists a summary of Tmax results. Temperature profiles are plotted for the top and bottom chips across the hot spot in Figure 20a and 20b respectively. The inset shows the approximate location of the plot data source from the contour plot for the top and bottom chips. These plots show that significant gradients and higher local temperatures occur due to hot spots. Alignment of hot spots on stacked chips produces the worst-case condition. The studies here show the effect of relatively large area hot spots. In practice, hot spots are likely to be much smaller and will further increase local temperatures and temperature gradients.

Table 7. Tmax and Thermal Resistance Results

Name	Tmax (°C)	θ_{JA} (°C/W)
Base Case	112.4	69.1
Top Case	112.8	69.9
Bottom Case	112.84	69.9
Both Case	113.6	70.6

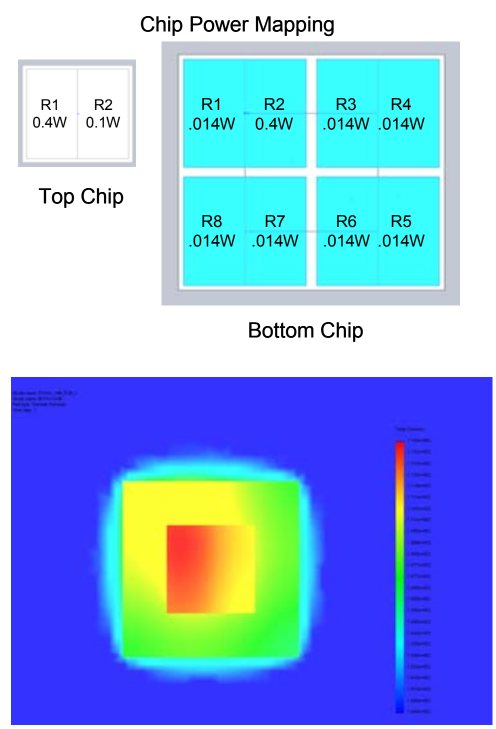


Figure 19. Both Case Power Map and Contour Plot

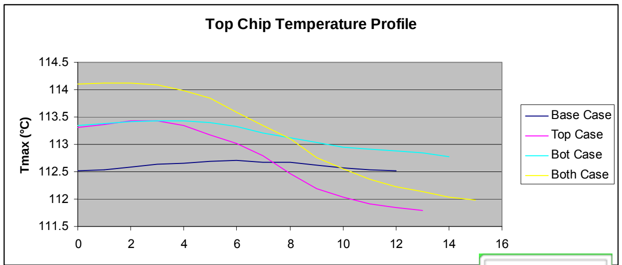
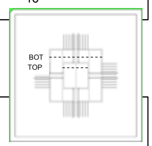


Figure 20a. Top Chip Profile



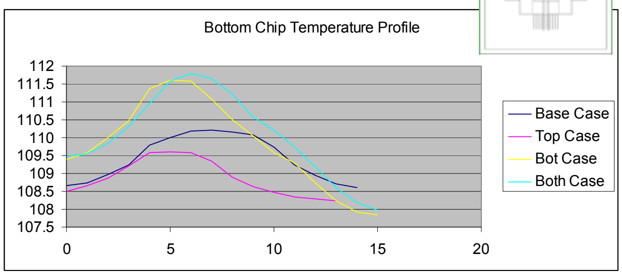


Figure 20b. Bottom Chip Profile

Conclusion

This study has shown that the use of dedicated test chips coupled with validated models can be used to understand temperature and heat transfer characteristics in stacked chip applications. Measurements and models are compared for the initial case showing a good representation of the assembly with straightforward and practical use of finite element software. The case studies show that the use of thermal test chips and modeling software can reveal information within the stacked die assembly which is not possible with live chips. The value of the test chip and validations will become more evident as more experiments are performed on the samples. Future work includes validation of hot spots by the use of multiple temperature sensors on the TTC to estimate the temperature distribution within a given unit cell. The experiments will be extended to the flip-chip version of the package and will be reported in future publications.

Acknowledgements

The authors wish to acknowledge the efforts of Mr. John McKay of SEMI-PAC for the package and test coupon assembly.

References

1. EIA/JEDEC Standard JESD15 Methodology for the Thermal Measurement of Component Packages, Standards JESD51-1, 51-2, 51-3, 51-4 and 51-5, Electronic Industries Association, JC15 committee, 1995.
2. B. Siegal, J. Galloway, "Thermal Test Chip Design and Performance Considerations", 24th Annual SEMI-THERM Symposium, 2008.
3. "Ball Grid Array Technology", J. H. Lau, Editor, Mcgraw-hill, Inc. 1995, ISBN 0-07-036608-X
4. K. Matsumoto, S. Ibaraki, K. Sueoka, K. Sakuma, H. Kikuchi, Y. Orii and F. Yamada, "Experimental Thermal Resistance Evaluation of a Three-Dimensional (3D) Chip Stack, 28th IEEE SEMI-THERM Symposium on Thermal Management, March 2011.
5. K. Matsumoto; K. Sakuma; F. Yamada; Y. Taira, "Investigation of the thermal resistance of a three-dimensional (3D) chip stack from the thermal resistance measurement and modeling of a single-stacked-chip", International Conference on Electronics Packaging, p.478, 2008.
6. B. Siegal, An Introduction to Diode Thermal Measurements, TEA Handbook, Thermal Engineering Associates, 2009.
7. T.-Y. Chiang; K. Banerjee; K. C. Saraswat,. "Analytical thermal model for multilevel VLSI interconnects incorporating via effect", IEEE ELECTRON DEVICE LETTERS, vol.23, p.31, 2002.
8. B. Zhan, "Evaluation of Simplified and Complex Thermal Fnite Element Models for a 3-die Stacked Chip Scale Ball Grid Array Package", 29th IEEE/CPMT/SEMI International Electronics Manufacturing Technology symposium, July, 2004.
9. Z. Celik, "Thermal Characterization of Various 2.5 and 3D Package Configurations for Logic and Memory Applications", MEPTEC 2.5D, 3D and Beyond: Bringing 3D Integration to the Packaging Mainstream seminar, MEPTEC/SEMI, November, 2011.
10. M. Janicki, A. Napieralski, J. H. Collet and A. Louri, "Hot Spots and Core-Core Thermal Coupling in Future Multicore Architectures", 26th Annual IEEE SEMI-THERM Symposium, March 2010.
11. T. Tarter, "Design of High Density & 3D Packaging: Tools and Knowledge", Presentation at IEEE/CPMT Technical Meeting, September 2010.
12. Thermal Engineering Associates, Inc. Technical Briefs, www.thermengr.net/TechBrief/.